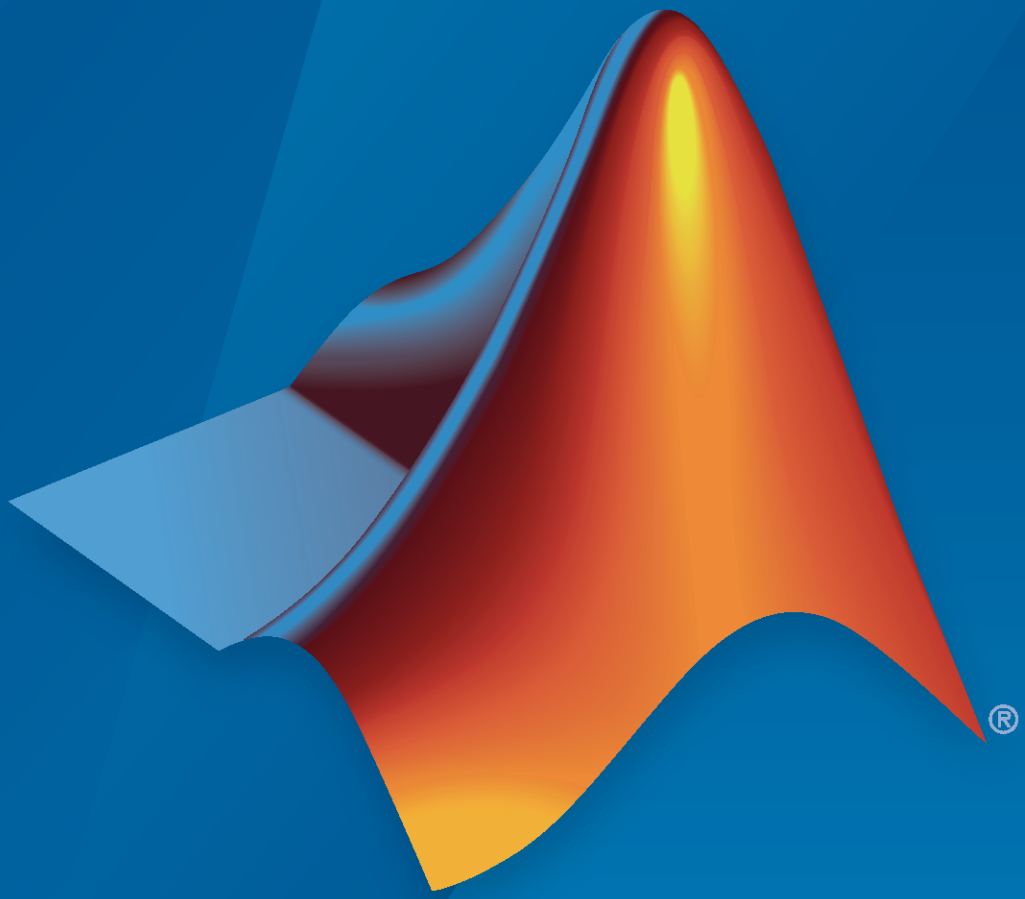
Signal Integrity Toolbox™

Reference



MATLAB®

R2021b

MathWorks®

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Signal Integrity Toolbox™ Reference

Revision History

September 2021	Online only	New for Version 1.0 (Release 2021b)

Contents

Apps

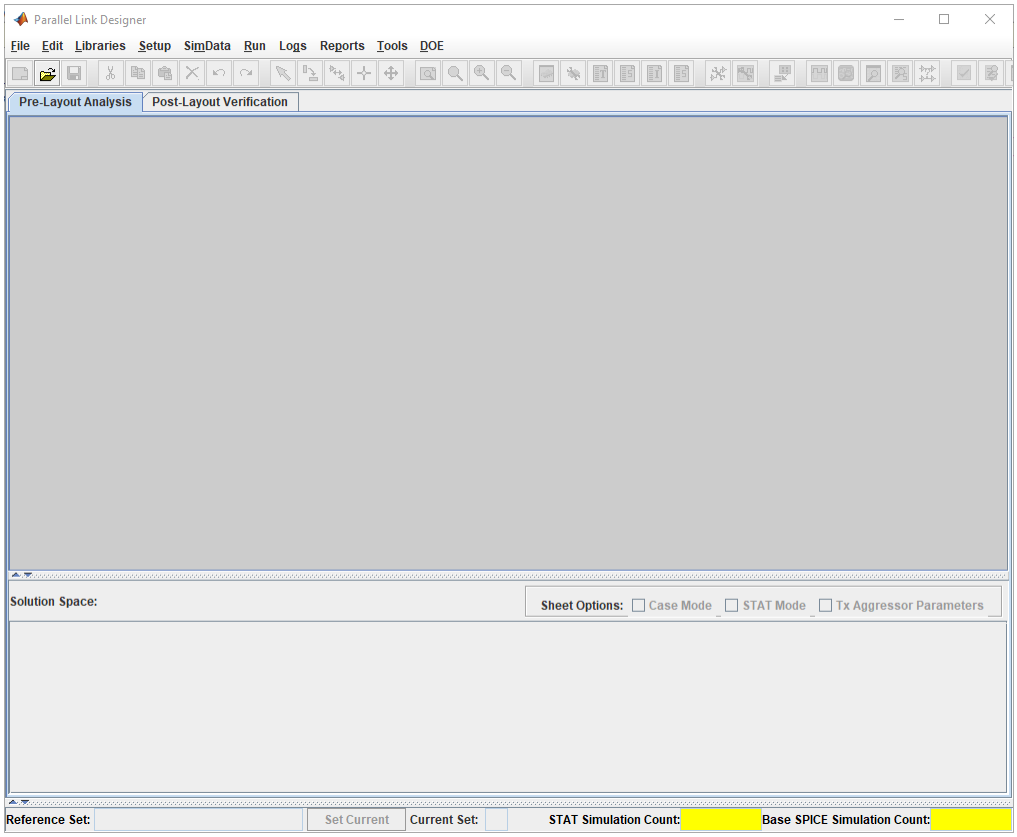
Parallel Link Designer

Analyze PCB designs for parallel link applications

Description

The **Parallel Link Designer** analyzes PCB designs for parallel link applications for both pre-layout and post-layout simulations. To perform post-layout analysis, you need a license for RF PCB Toolbox™.

Using pre-layout analysis, you can determine system-level noise and timing margins from integrated signal integrity, waveform, timing, and crosstalk analysis. The pre-layout analysis environment generates design guidelines for your board layouts, package layouts, connectors, and cabling. The post layout environment verifies the actual layout against the design guidelines.



Open the Parallel Link Designer App

- MATLAB® Toolstrip: In the **Apps** tab, under **Signal Processing and Communications**, click the app icon.
- MATLAB command prompt: Enter `parallelLinkDesigner`.

Examples

- “Analyze Parallel Links with Parallel Link Designer”
- “Configure DDR2 Controller with Two Memory Designators”

Programmatic Use

`parallelLinkDesigner` opens a new session of the **Parallel Link Designer** app, enabling you to design and analyze a parallel link.

`parallelLinkDesigner(path/file.edk)` opens the interface designed by the file.

`parallelLinkDesigner(file.script)` runs a script file and returns the app process handle.

More About

Simulation Parameters

Simulation Parameters control how the analysis is run in the **Parallel Link Designer** app. For detailed information about them, see “Simulation Parameters Used in Parallel Link Design”.

Corner Conditions

There are two types of corner conditions you can vary using the **Parallel Link Designer** app.

- IC Environment Corners — These are the temperature parameter for each corner. They do not affect IBIS buffer models.
- Etch Corners — These are the scaling factors for the Z_0 and T_{pd} parameters of transmission line models. Both ideal and lossy transmission line models are scaled. Lossy transmission line models are scaled by computing the values of Z_0 and T_{pd} from the typical corner L and C values.

For more information, see “Specify Corner Conditions in Parallel Link Design”.

Stimulus Patterns

You can specify the stimulus patterns for the time domain analysis. If the specified pattern for a designator has fewer bits than the simulation length, the pattern is repeated from the first bit of the pattern. If the pattern is longer than the simulation length the simulation will end at the time specified by **Time Domain Stop**. For more information, see “Stimulus Patterns in Parallel Link Design”.

Widebus (Pre-Layout Crosstalk Analysis)

In **Parallel Link Designer** app, pre-layout crosstalk analysis is referred to as widebus crosstalk analysis. It consists of single transfer sheets (transfer nets) and a “widebus” or coupled sheet with a victim transfer net and one or more aggressor nets.

Each unique transfer net on a widebus schematic sheet is known as a “widebus group”. That group consists of ONLY the transfer net designators (drivers, receivers or I/O buffers). On a widebus sheet any widebus group can be a victim or aggressor and multiple instances of any widebus group can be placed on the schematic. The widebus groups inherit the designator properties defined in their

transfer net sheet. Coupled w-lines, connectors, package models or s-parameter blocks can then be used in the widebus schematic to connect up each widebus group. One of the instances of a widebus group will be designated as the victim net on the schematic.

Each unique transfer net on a widebus schematic sheet is known as a “widebus group”. That group consists of ONLY the transfer net designators (drivers, receivers or I/O buffers). On a widebus sheet any widebus group can be a victim or aggressor and multiple instances of any widebus group can be placed on the schematic. The widebus groups inherit the designator properties defined in their transfer net sheet. Coupled w-lines, connectors, package models or s-parameter blocks can then be used in the widebus schematic to connect up each widebus group. One of the instances of a widebus group will be designated as the victim net on the schematic.

Widebus analysis can be performed on any project, even previous incarnations of a design. The following requirements are:

- One or more reference transfer nets (sheets) exist. The designator grouping on each unique transfer net are referred to as a “widebus group”.
- Each transfer nets consist of a single driver per transfer (they can have multiple transfers (i.e. memory read/memory write), and can have multiple receivers/loads.
- Transfer net characteristics such as transfers, UI, type, probe points and jitter are defined in the transfer net characteristics (not on a widebus sheet).

To create a widebus sheet there must be at least one transfer net included in the schematic set. Select **File > Schematic Sheet > New Sheet** from the app toolbar. In the newly opened New Sheet dialog box, select **Widebus** and select the widebus groups to be added to the sheet and the number of instances of each.

Clock Forwarding

The **Parallel Link Designer** app supports the clock forwarding methodology defined in IBIS BIRD 204. This BIRD describes a mechanism by which the clock waveform, or recovered clock times, can be passed to the data AMI receiver model to allow the model maker access to the clock. This enables the receiver model to include clock phase noise, clock tree delays, phase interpolators, etc. IBIS BIRD204 has been approved by the IBIS committee and will be included in the IBIS 7.1.

A serial-link channel uses a CDR (clock data recovery) circuit in the receiver to create a clock signal that is then used to latch each individual data bit coming into the core of an IC. The IBIS-AMI standard was created to model this operation and a CDR is required to be present, either in the receiver model itself (the norm) or in the EDA tool that is running the simulation. By contrast, in a parallel-link channel no CDR is present. Instead, a separate clock (or strobe) signal is sent along with the data signals, which is used to latch sets of data bits at one time. This is known as clock-forwarding.

Clock forwarding is accessed by selection of a clock group in the Widebus Groups dialog box. The clock group identifies the clock and which respective data signals are associated with it. This relationship is used for analyzing clock recovery in the parallel interface.

Any widebus group transfer net that has been set up as a clock or strobe will be considered to be a clock group on the widebus sheet. The clock group drop down menu selection will show all strobe/clock groups on the current widebus sheet, plus "<none>". Clock transfer nets will default to “<none>”. Data transfer nets will default to first clock or strobe associated sheet. Each data group can be associated with a different clock group which also supports sweeping of victim group.

See Also

Apps
SI Viewer

Topics
“Analyze Parallel Links with Parallel Link Designer”
“Configure DDR2 Controller with Two Memory Designators”

Introduced in R2021b

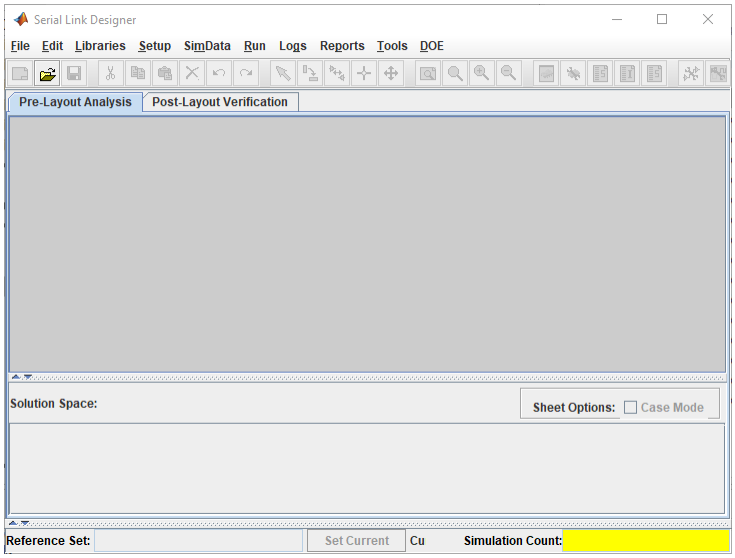
Serial Link Designer

Analyze PCB designs for serial link applications

Description

The **Serial Link Designer** app analyzes PCB designs for serial link applications for both pre-layout and post-layout simulations. To perform post-layout analysis, you need license to RF PCB Toolbox.

Using pre-layout analysis, you can determine system-level noise and timing margins from integrated signal integrity, timing, and crosstalk analysis. The pre-layout analysis environment generates design guidelines for your board layouts, package layouts, connectors, and cabling. The post-layout environment verifies the actual layout against the design guidelines.



Open the Serial Link Designer App

- MATLAB Toolstrip: In the **Apps** tab, under **Signal Processing and Communications**, click the app icon.
- MATLAB command prompt: Enter `serialLinkDesigner`.

Examples

- “Analyze Serial Links with Serial Link Designer”
- “Analyze Backplane with Line Cards”
- “Edit Imported S-Parameter Data”

Programmatic Use

`serialLinkDesigner` opens a new session of the **Serial Link Designer** app, enabling you to design and analyze a serial link PCB.

`serialLinkDesigner(file.qcd)` opens the interface designed by `file.qcd`.

`serialLinkDesigner(file.script)` runs a script file and returns the app process handle.

More About

Simulation Parameters

Simulation Parameters control how the analysis is run in the **Serial Link Designer** app. For more information, see “Simulation Parameters Used in Serial Link Design”.

Corner Conditions

There are two types of corner conditions you can vary using the **Serial Link Designer** app.

- IC Environment Corners — These are the temperature parameter for each corner. They do not affect IBIS buffer models.
- Etch Corners — These are the scaling factors for the Z_0 and T_{pd} parameters of transmission line models. Both ideal and lossy transmission line models are scaled. Lossy transmission line models are scaled by computing the values of Z_0 and T_{pd} from the typical corner L and C values.

For more information, see “Specify Corner Conditions in Serial Link Design”.

Stimulus Patterns

You can specify the stimulus patterns for the time domain analysis. If the specified pattern for a designator has fewer bits than the simulation length, the pattern is repeated from the first bit of the pattern. If the pattern is longer than the simulation length, the simulation will end at the time specified by **Time Domain Stop**. For more information, see “Stimulus Patterns in Serial Link Design”.

See Also

Apps
SI Viewer

Topics
“Analyze Serial Links with Serial Link Designer”
“Analyze Backplane with Line Cards”
“Edit Imported S-Parameter Data”

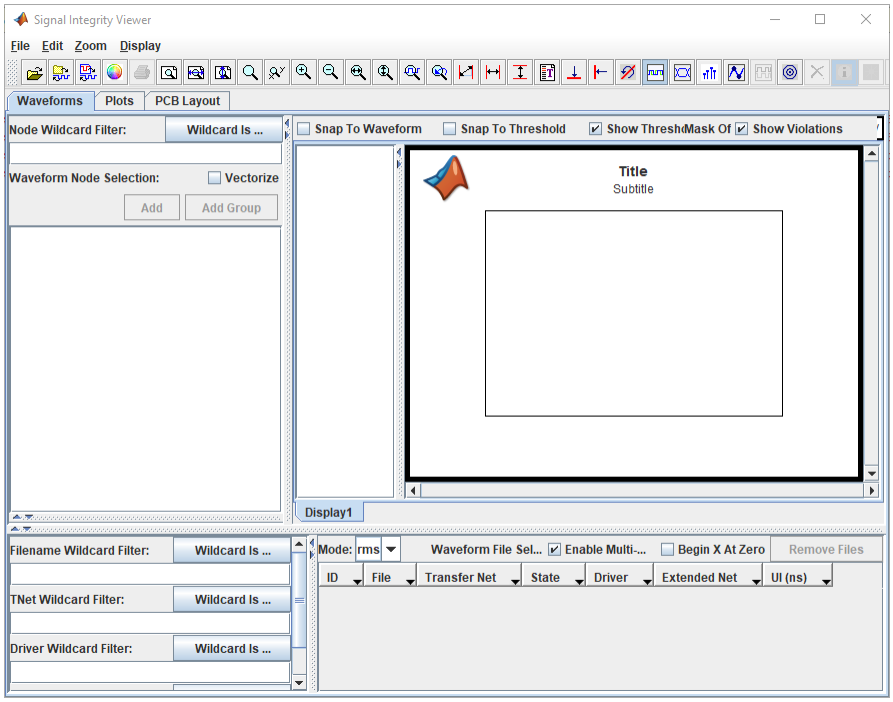
Introduced in R2021b

Signal Integrity Viewer

View the signal integrity results of Serial Link Designer or Parallel Link Designer app

Description

Use the **Signal Integrity Viewer** app to view the results of the simulations done in **Serial Link Designer** or **Parallel Link Designer** app. This app displays waveforms, eye diagrams, and other visual formats produced by the two apps.



Open the Signal Integrity Viewer App

- MATLAB Toolstrip: In the **Apps** tab, under **Signal Processing and Communications**, click the app icon.
- MATLAB command prompt: Enter `signalIntegrityViewer`.

Examples

- “Analyze Serial Links with Serial Link Designer”
- “Analyze Parallel Links with Parallel Link Designer”

Programmatic Use

`signalIntegrityViewer` opens a new session of the **Signal Integrity Viewer** app, enabling you to view the results of a serial link or parallel link analysis.

`signalIntegrityViewer(file.csv)` opens the waveform files. Waveform files can be `.csv` or `.tr0` files from HSPICE.

`signalIntegrityViewer(file.cfg)` opens a saved configuration file.

More About

Reports in Serial Link Designer

The **Signal Integrity Viewer** app generates validation reports, netlist generation reports, and channel analysis reports among various reports, results, and waveforms. For more information, see “Results of Pre-Layout Analysis in Serial Link”.

Reports in Parallel Link Designer

The **Signal Integrity Viewer** app generates validation reports, waveform and timing reports, SPICE generation reports, and assignment reports among various reports, results, and waveforms. For more information, see “Results of Pre-Layout Analysis in Parallel Link”.

See Also

Apps
Serial Link Designer | **Parallel Link Designer**

Topics
“Analyze Serial Links with Serial Link Designer”
“Analyze Parallel Links with Parallel Link Designer”

Introduced in R2021b